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Dual Input Logic AND Device Fabricated Using an *n*-doped Semiconductor: Effects of UV Light on Charge Mobility

Alexander O. Rosado
Department of Physics and Electronics
University of Puerto Rico at Humacao
Humacao, PR 00792

Faculty Advisor: Dr. Nicholas Pinto

Abstract

An *n*-doped ActivInk™ N2200 [P(NDI2OD-T2)] thin-film transistor having a dual split gate architecture has been fabricated on a doped silicon/silicon dioxide (Si/SiO_2) substrate. This device demonstrates AND logic functionality which was controlled by applying either 0 or 50V to each of the gate electrodes. When 50V was simultaneously applied to both gates, the device was conductive (ON state) while any other combination of gate voltage rendered it resistive (OFF state). We tested the device in the presence of ultra-violet (UV) light and measured a higher mobility compared to the absence of UV. A possible explanation is that electron trapping adsorbate groups on the P(NDI2OD-T2) surface (possibly O_2^- or H_2O^-) inhibit charge transport. Upon UV exposure, an electron-hole pair is generated that liberates the adsorbates via hole recombination ($h^+ + O_2^- \rightarrow O_{2\,(gas)}$) releasing electrons that contribute to charge transport. The *n*-type carrier charge mobility was 2×10^{-6} $cm^2V^{-1}s^{-1}$ upon UV exposure, meanwhile without UV exposure it was $3.3 \times 10^{-7} cm^2V^{-1}s^{-1}$. The low mobility of these devices was due to the rough surface of the substrate. An advantage of this architecture is the possibility of having multiple inputs with a single P(NDI2OD-T2) channel and also its ability to sense UV radiation.

Keywords: ActivInk^{TM}, FET, Polymer, UV

1. Introduction

Ever since the discovery of conducting polymers[1], intense research has been focused on the charge transport properties and to integrate them in devices. These devices include organic field-effect transistors (FET) and sensors that also have multifunctional capabilities. Organic conducting polymers have made it possible to design reliable and inexpensive devices and sensors under ordinary laboratory conditions. Initially, only organic *p*-doped semiconducting polymers could be synthesized because organic *n*-doped semiconductors were readily oxidized in air and, hence, inoperative. In recent years, however, an air stable *n*-doped semiconductor poly{[N, N'bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)} [P(NDI2OD-T2)] was synthesized[2]. Most FET's that incorporate this polymer as the active channel use a *single* (global) gate. In this paper we use the above semiconductor in a *split dual gate* FET architecture (where each gate can be independently addressed) in combination with a single channel between the source and drain electrodes. To the best of our knowledge, this is the first time [P(NDI2OD-T2)] has been reported with such a dual gate architecture.

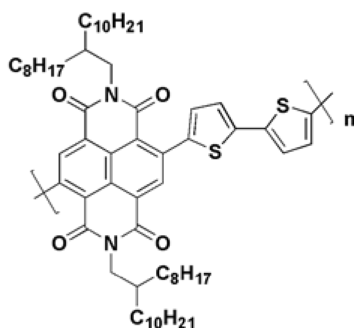

Figure 1. Molecular structure of the *n*-doped [P(NDI2OD-T2)] polymer[3].

Figure 1 above shows the chemical structure of P(NDI2OD-T2)[3]. Organic semiconductors in general, whether *p*-doped or *n*-doped, have a propensity to have low mobility; therefore, any actions that enhance the mobility of these semiconductors are keenly sought. One way to improve the mobility is to use ultraviolet radiation [4]. Our results show that ultraviolet (UV) light exposure, (*i*) enhances mobility, (*ii*) increases the current on/off ratio and (*iii*) the device still maintains he same logic A.N.D. gate properties measured in the absence of UV light. Molecular adsorption of electron trapping species and photo-excitation are suggested as possible explanations for these effects, as it is related to the decrease of charge traps leading to an increased mobility. The results of this experiment are reproducible and have shown that UV irradiation can enhance FET parameters.

2. Experimental Methods

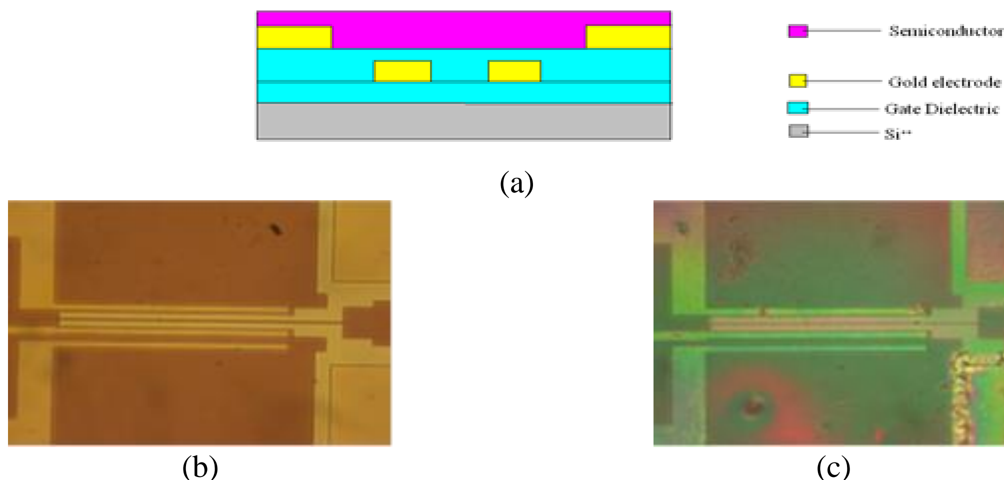

Figure 2. (a) Schematic of our split-gate FET. Images of the device surface (b) before and (c) after the [P(NDI2OD-T2)] deposition.

The dual split gate architecture of the device consists of a source and drain electrode over a layer of silicon dioxide (SiO_2) with two gate electrodes underneath the SiO_2 layer, as shown in Figure 2(a). Access to the gate electrodes was obtained by etching windows into the SiO_2. Another SiO_2 layer lies beneath the two gate electrodes with a silicon (Si^{++}) base. The fabrication of our device consisted of a thin-film of a drop of octadecyltrichlorosilane (OTS) in 5 ml of hexane and air dried at 80° C for 24 hours. A 0.5wt% solution of the *n*-doped [P(NDI2OD-T2)] in dichlorobenzene was spun-coated over the layer of the OTS coated substrate and air dried at 100°C. This OTS thin-film provides a hydrophobic surface and allows a better adhesion of the n-doped semiconductor. Figures 2(b) and

2(c) shows the surface of our device before and after spin-coating [P(NDI2OD-T2)]. Illumination of ultraviolet light was provided by a model UVGL-25 lamp of wavelength 365nm and a fixed intensity of 720 $\mu W/cm^2$.

3. Results and Discussion

The plot of the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) of a [P(ND12OD-T2] spin coated thin film FET at four combination sets of gate 1 and gate 2 biases (V_{GS}) in the absence of UV light is shown on Figure 3(a).

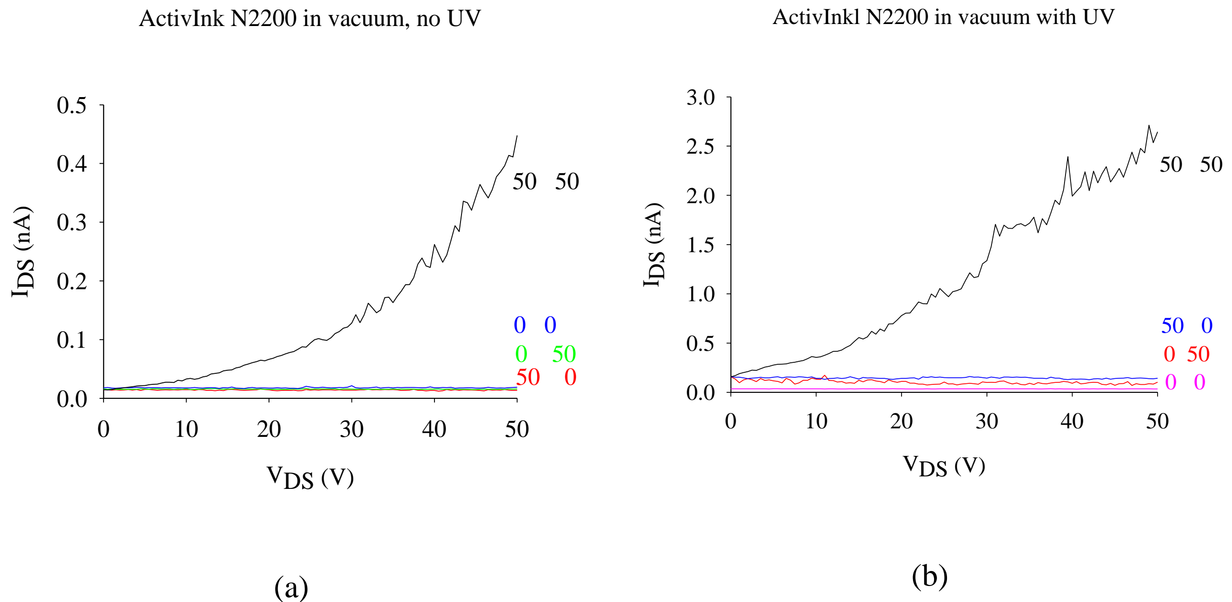

Figure 3. Drain-source current versus drain-source voltage (I_{DS}-V_{DS}) characteristics in absence of UV light where the gate voltages V_{GS1} and V_{GS2} are as indicated to the right of the plot. When the gate bias is 50V 50V the device is ON, while any other combination, the device is OFF. (a) In the absence of UV (b) in the presence of UV. Note the higher measured currents in the presence of UV.

When the bias voltage applied to gate 1 and gate 2 is 50V, the measured channel current increased with rising positive drain-source bias. This implies the ON state for the device. At 0V in gate 1 and/or gate 2 biases, the channel current remained low and unchanged with increasing drain-source bias. This implies the OFF state for the device. As seen in figure 3(b), upon UV irradiation, the channel current is higher for all gate 1 and gate 2 combinations, implying increased device on/off ratio and charge mobility. This increase in channel current is most likely due to photo-excitation of charge from the valence into the conduction band of the polymer and also due surface charge doping which results from desorption of electron trapping species. Since the device was handled in air, it is likely that electron trapping groups like O_2- or H_2O- were adsorbed on the polymer surface. Upon UV exposure, an electron-hole pair is generated that liberates the adsorbates via recombination with holes (*e.g.* $h^+ + O_2^- \rightarrow O_2$ (gas)) on both sides of the polymer surface, releasing electrons that then contribute toward the increase in the observed current. As can be seen in Figures 3(a) and (b), at 0V gate 1 and/or gate 2 bias the channel current of the device remained unchanged upon UV light exposure. This means that the device's logic A.N.D. properties were unaffected upon UV irradiation.

An important device parameter indicative of performance is the charge mobility. From the data presented in Figures 3 we can extract first the device transconductance (g_m) using the formula[5]:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \text{ with } V_{DS} = \text{constant} \quad (1)$$

Given that V_{GS1}=V_{GS2}=50V and V_{DS} =50V, g_m is calculated to be 8.5 x 10^{-12} S in the absence of UV light while in the presence of UV light, g_m is calculated to be 5.22 x 10^{-11} S. From these values of g_m we calculated the carrier mobility (μ) using the formula[4]:

$$\mu = \frac{g_m L}{W C_i V_{DS}} \quad (2)$$

where g_m is the transconductance calculated using Eq. (1), L (40μm) is the channel length, W (600μm) is the channel width, C_i is the capacitance per unit area of the 300nm thick silicon dioxide layer (3.45 x 10^{-8} F/cm^2) and V_{DS} is the constant drain-source voltage (50V). In the linear region, the mobility without UV radiation is calculated to be 3.3 x 10^{-7} cm^2/V-s while in the presence of UV it is 2 x 10^{-6} cm^2/V-s. These values of charge mobility are small compared to that of amorphous silicon and need to be improved upon. The device ON/OFF ratio, defined as the ratio of the currents when the gate bias was 50V (ON) and 0V (OFF) at a fixed V_{DS} of 50Vis also seen to increase in the presence of UV.

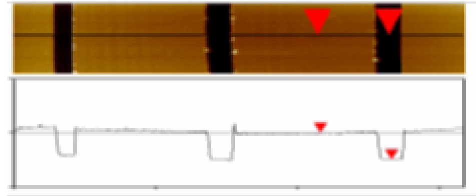

Figure 4. Atomic Force Microscope image of a section of the device substrate as seen in Figure 2(b). The plot below is the height profile along the dark line seen in the AFM image above. The rad arrows indicate that the substrate is not planar.

One reason for these small mobility values is the substrate topography which is not planar as seen in Figure 4 due to the buried gate electrodes which leave sharp edges. These edges unfavorably affected the charge mobility leading to suboptimal device characteristics. Efforts will be made in the future to further study and improve the device parameters via the use of an ultraviolet lamp whose intensity can be varied.

4. Conclusions

We successfully fabricated a dual split gate FET using the *n*-doped [P(NDI2OD-T2)] semiconductor. The device was conductive when 50V were simultaneously applied to both gates. Any other combination of gate voltages rendered the device resistive. Thus the device behaves as a dual input logic A.N.D. gate. In absence of UV light, the device exhibits a mobility of 3.3 x 10^{-7} cm^2/V-s with a current ON/OFF ratio of 28. When exposed to UV light the device parameters improved i.e. the device mobility increased to 2 x 10^{-6} cm^2/V-s and its ON/OFF ratio increased to 77. The ability to function as a logic A.N.D. gate and also detect UV light makes this device multifunctional and very useful in electronic applications in outer space where UV radiation levels are high.

5. Acknowledgements

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6. References

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