Proceedings of the National Conference
On Undergraduate Research (NCUR) 2016
University of North Carolina Asheville
Asheville, North Carolina
April 7-9, 2016

Crossing Waveguides in Silicon-Based Optical Devices

Jimmy Yin
Department of Electrical Engineering and Computer Science
Photonics Research Center
Bartlett Hall, Bldg. 753 ATTN: MADN-PRC
West Point, NY 10996 USA

Faculty Advisor: LTC Brian Souhan

Abstract

Moore's Law states that silicon chip performance will double approximately every 18 months. However, as transistor size approaches the physical limits of fabrication, researchers are looking into photonic integrated circuits as the new path forward. Silicon waveguide crosses are an essential component for high-density photonic integrated circuits. The crosses must be highly compact, yet highly efficient. Previous works have proposed low insertion loss and low crosstalk waveguide crossings, however, the crosses remain relatively large at 6x6 microns. A new proposal discussed a waveguide crossing where insertion loss and crosstalk remain low, but the size is greatly reduced to 1x1 microns. The size reduction is achieved by a small, lens-like structure at each terminal of every cross. While simulations show an insertion loss less than 0.18dB and crosstalk less than -30dB, fabricated crosses have not been tested in a laboratory setting. This research attempts to fabricate the proposed devices on a silicon chip using electron beam lithography and take crosstalk and insertion loss measurements. Measurements were performed using a test setup composed of three stages capable of five axis manipulation for fiber and chip alignment, two lens tapered fibers for coupling light onto the chip, a polarization rotator to control polarization of the input light, a tunable light source producing 1550nm light, and an optical spectrum analyzer for measuring power. Insertion loss was measured by using the cutback method, comparing straight waveguides consisting of varying number of waveguide crossings. Preliminary results show an approximate 0.52 dB insertion loss per crossing. The higher than expected loss compared to simulation is likely due to deviations in the lens dimensions related to proximity effect, common to e-beam lithography. Continued work will focus on gathering more data from the current fabricated devices and fabricating additional devices that account for the proximity effect.

Keywords: Crossing Waveguides, Silicon, Insertion Loss

1. Introduction

Moore's Law states that silicon chip performance is expected to double about every 18 months. As researchers begin to reach the limits of transistor fabrication on the nanometer scale, they have begun looking toward using integrated circuit photonics to circumvent transistor limitations. Silicon waveguide crosses are an essential component for high density photonic integrated circuits. Waveguide crosses effectively halves the required vertical footprint of two independent waveguides.

A silicon waveguide crossing is composed of two waveguides on the same vertical axis. Referencing the cross in Figure 1(a), one signal can travel on the x-axis waveguide while another signal can travel on the y-axis waveguide with little interaction between the two signals. For perfect transmission, the signal traveling through the waveguide experiences no attenuation as it propagates through the waveguide (zero insertion loss) and no leaks into the crossing waveguide (zero crosstalk). If sufficiently low crosstalk and low insertion loss can be achieved, it would allow for the rapid development of photonic integrated circuits. Current research characterizes high performing crosses as those

with sub 0.2dB insertion loss and -40dB crosstalk [1]. A 90˚ waveguide crossing with no modifications to either waveguide has a crosstalk similar to 12dB.

2. Background

Various researchers have attempted to reduce the size of waveguide crosses through a variety of methods, such as changing the angle of the cross [2] and tapering the terminals of the cross [1,4]. In a paper published by Ma et al. in 2013, they were able to demonstrate a 9 µm x 9 µm crossing waveguide using a tapered structure [1]. These crosses had an insertion loss of -0.028 ± 0.009 dB and a crosstalk of less than -37dB.

As shown in Figure 1(a), 9 µm is measured from the beginning of the expanding cross (where w1 is located) to the termination of the cross on the other end (where w1 would be located on the opposite side). While this structure exhibits excellent performance metrics, its 9 µm x 9 µm footprint is much too large for high-density photonic integrated circuits.

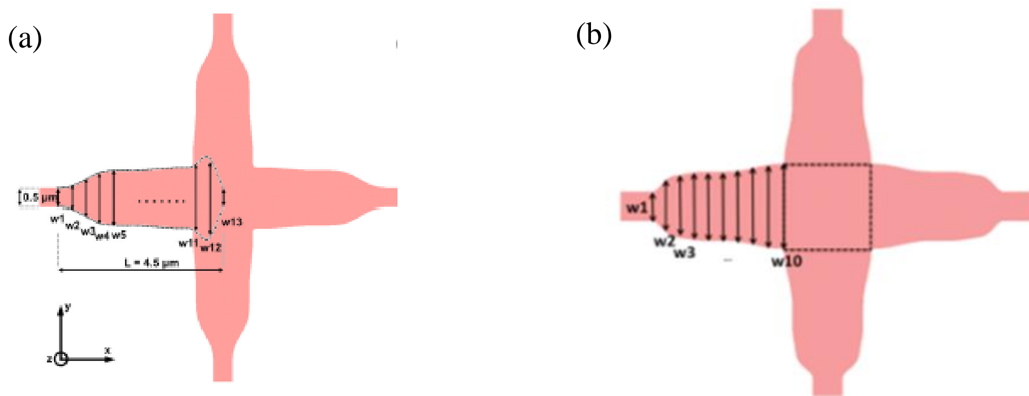
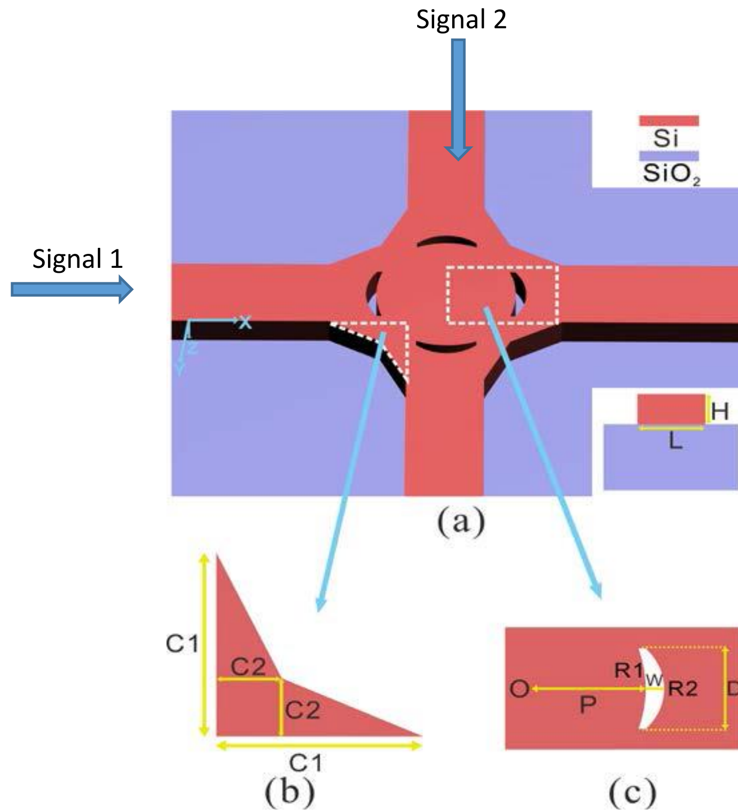


Figure 1. (a). Structure of cross in Ma *et al*. [1]. (b). Structure of cross in Zhang *et al*. [4].

Zhang et al. also published a paper in 2013 detailing a 6 µm x 6 µm crossing structure with an insertion loss of 0.18 ± 0.03 dB and a crosstalk of -41 ± 2 dB [4]. The structure is very similar to the one mentioned above, however, it still has a very large footprint that is unsuitable for high density photonic integrated circuits.



Waveguide Crossing Structure Parameters (μm)								
C1	C2	P	R1	R2	D	W	H	L
0.26	0.094	0.382	0.459	0.2	0.28	0.06	.250	0.50

Figure 2. Cross structure using integrated nano-lenses, proposed by Ming Dai et al [5].

In their unpublished paper, Ming Dai et al. [5] proposed a highly compact waveguide suitable for photonic integration. The proposed crossing structure brings the size of the cross down to 1 μm x 1 μm. The size reduction is achieved through a small lens-like structure at every terminal of each cross, as shown in Figure 2. The dimensions are also shown in Table 1 [5].

Their paper details finite-difference time-domain simulations that show crosstalk to be less than -30 dB and insertion loss of less than 0.18 dB. Simulations were used to investigate the cross's tolerance to fabrication variation among five geometric parameters: P, R1, R2, L, and W. Results found that this crossing structure, in simulations, is highly tolerant to fabrication variations, with transmitted power declining to 94.5%, which translates to an insertion loss of 0.246 dB per cross.

3. Characterization of Crosses

The focus of this research was on creating the test setup, ensuring it would be possible to characterize the crosses and taking insertion loss measurements. Although possible to take other measurements, insertion loss is the best indicator of whether the lenses achieve the desired effect.

3.1. Device Fabrication

The chips discussed in this paper were fabricated at Brookhaven National Laboratory. The chips are based on a SOITEC SOI wafer, consisting of a 600 μm layer of Si, a 3 μm layer of SiO2, and a 220 nm top layer of silicon. Using electron-beam lithography, the waveguides are etched to the desired patterns.

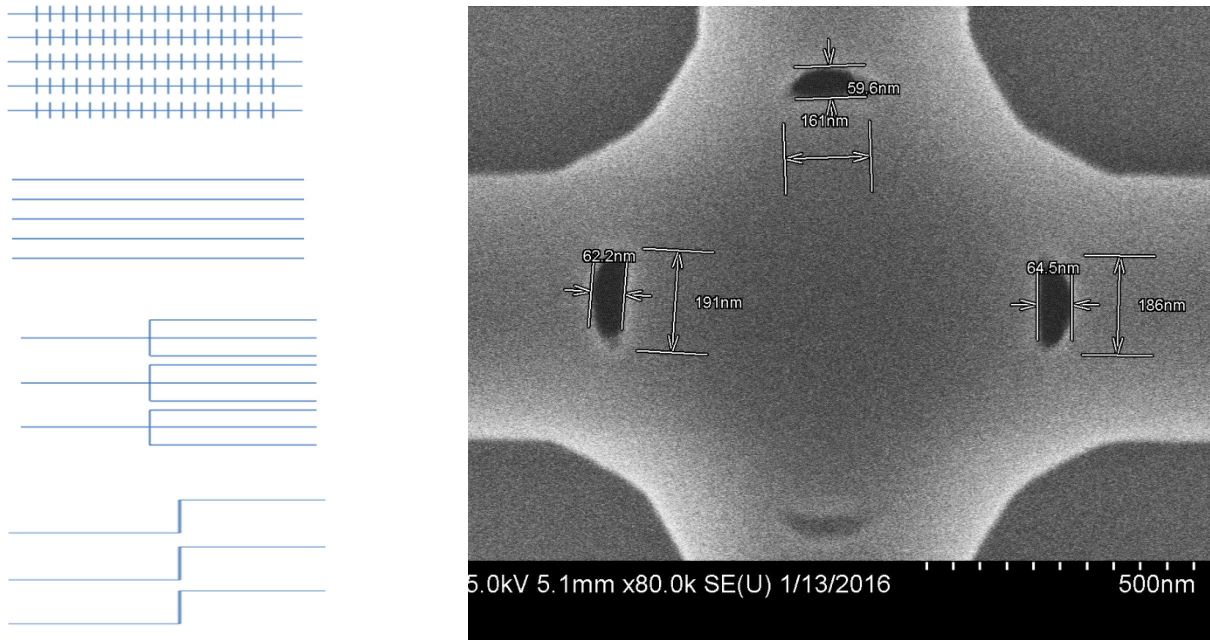


Figure 3. (a). Layout of the different test structures, starting with the crosses at the top, followed by straight waveguides, then crosstalk structure, with the final set for measuring loss through bends. (b). SEM image of a cross on a fabricated device.

Figure 3(a) shows the waveguide structures etched, with each set of waveguides used to measure a different parameter. The first set of waveguides each have 19 crosses with the lens structure present (as seen in the Figure 3(b). The straight waveguides are used to determine the system losses without the crossings. The third set of waveguides are to take crosstalk measurements. The fourth set of waveguides are used to determine the loss associated with bends in the waveguide.

Figure 3(b) shows an SEM of the fabricated cross structure with the lenses. Although the width (W) of the lenses are close to the nominal value, the length (D) appears significantly less than desired. Additionally, although the outer portion of the lenses appear well shaped, the inner portions appear more flat than curved. These inconsistencies are believed to be due to the proximity effect, a common occurrence in nanoscale lithography [6]. Finally, it is noted that the crosses along the horizontal direction (light propagation direction) were consistently better formed than those aligned along the vertical direction. This may be related to how the design software fractured the pattern for electron-beam writing and are currently working on fracturing the patterns differently to improve consistency amongst the different directions.

3.2. Chip Preparation

When the chips are first fabricated, the waveguides are all etched in the middle of the silicon chip. To prepare the chip for testing purposes, we cleave the silicon chips to expose the coupling portion of waveguides. The coupling portion of the waveguides consisted of a 3.85 μm wide section that was then adiabatically tapered down to the 500 nm wide waveguide. Using a diamond-tipped chip etcher, we carefully etch both ends of the chip, then cleave the chip, giving us access to the waveguides. An example of a cleaved chip is shown below in Figure 4.

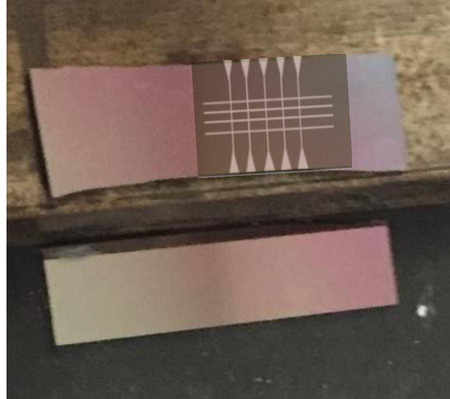


Figure 4. Image of a cleaved chip. The cleaving method provides a clean surface at the coupler interface for coupling light into the chip.

3.3. Test Setup and Methodology

The test setup composed of three stages capable of five axis manipulation, the ThorLabs NBM513/M, for fiber and chip alignment, two lens tapered fibers for coupling light onto the chip, a polarization rotator, the ThorLabs FPC560, to control polarization of the input light, a tunable semiconductor light source, a Santec TSL-510 producing 1550nm light, and an optical spectrum analyzer, a Yokogawa AQ6375, for measuring power, as show in Figure 5.

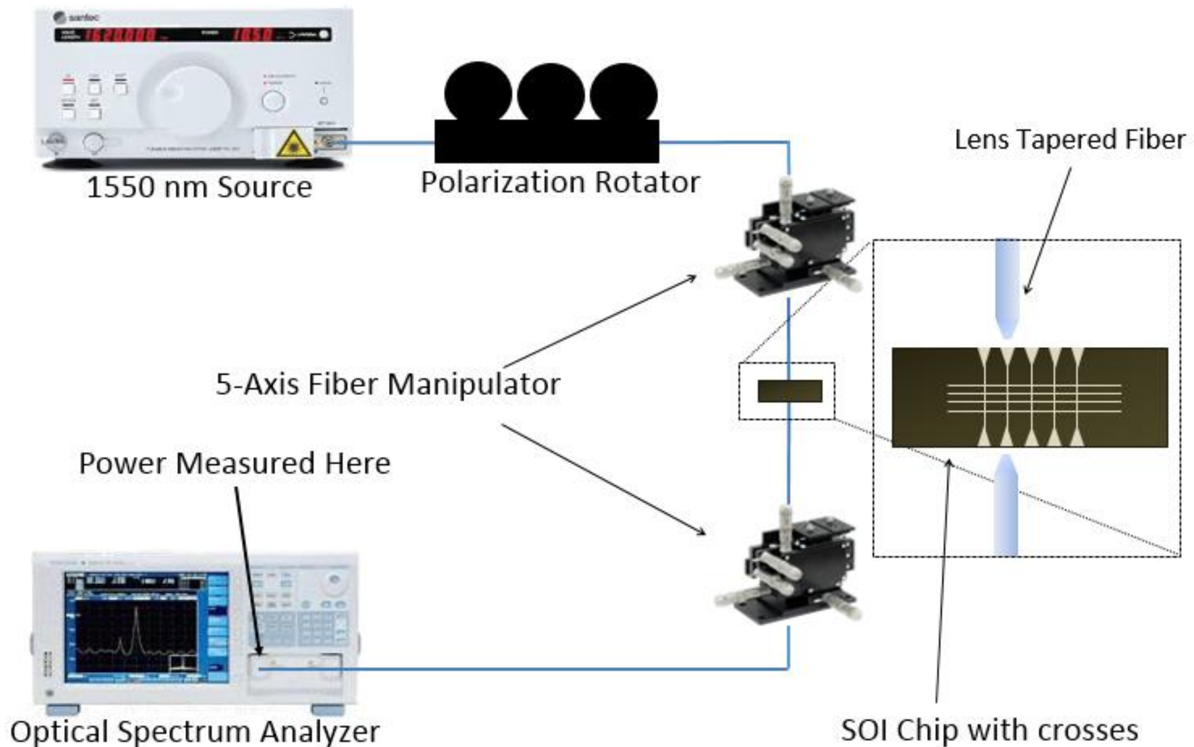


Figure 5. Block diagram of measurement setup.

The two stages holding the fiber tips use the ThorLabs HFG001 Fiber chucks. Additionally, we use a 3D printed a stage extender that we designed for the stage holding the chip. This stage extender allowed us to move the fiber stages closer together, reducing vibrations at the lens-tapered fiber tips. The stage extender with a chip on top is shown in Figure 6. Figure 7 shows the test setup that includes all three stages, the stage extender, and the microscope that aids in alignment of the fiber tips to the waveguide.

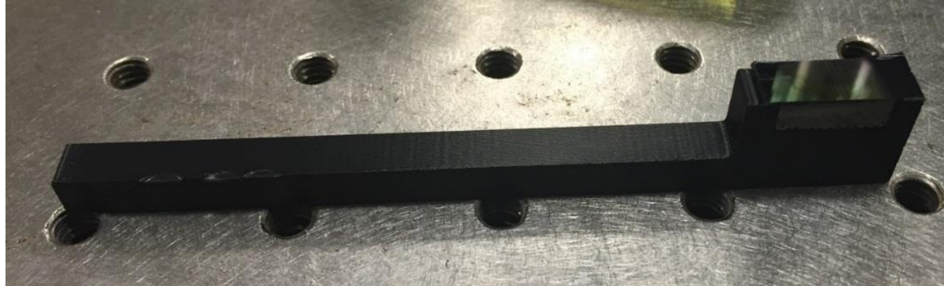


Figure 6. 3D Printed stage extender to hold chip in proper position and at proper height.

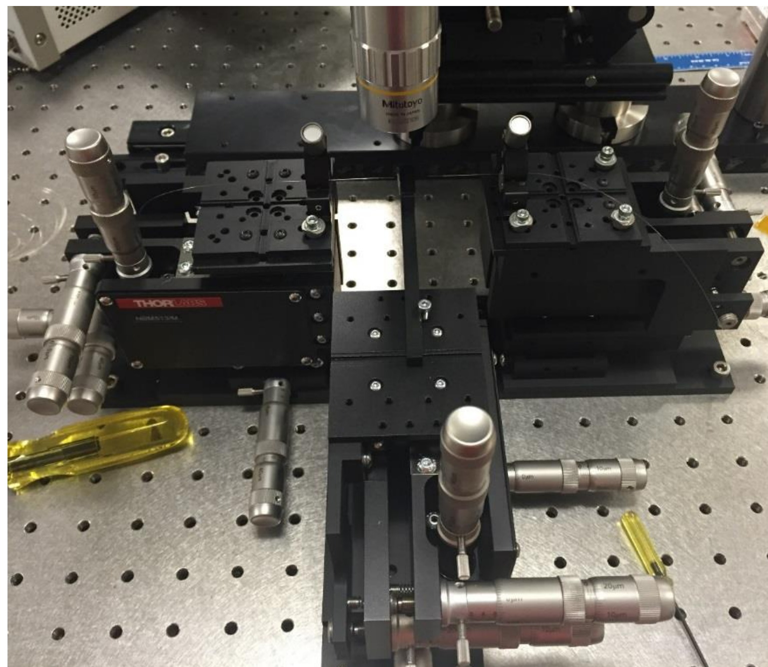


Figure 7. Test measurement setup

Using the cutback method, power measurements are taken as the light travels through one of the straight waveguides. Once the fibers were aligned on both sides of the waveguide, the 1550nm light was coupled through the waveguide and the output power was shown on the OSA. Once the power was maximized by adjusting the polarizer and fine tuning the fiber alignment, the process is then repeated on a waveguide with the crosses present. Holding all other variables constant, the only variation is the number of crosses on the waveguide. With a known number of crosses and the power through both waveguides, the insertion loss for each cross can be calculated, assuming each cross is nearly identical.

4. Results and Discussion

Preliminary results showed an overall insertion loss of roughly 9 dB per 19 crosses, which amounts to 0.47 dB per cross. Our coupled power into the waveguides varied greatly from day to day. Depending on our coupling efficiency, the measured power could vary from 1 μW to 10 μW. Regardless of coupling efficiency, the difference between a waveguide with no crosses and a waveguide with 19 crosses was around 10dB. The most common value was 2 ± 0.75 μW from the straight waveguides and 0.25 ± 0.08 μW from the waveguides with 19 crosses.

All the data taken so far was only on one of the two test chips available. No attempts have yet been made to couple light into the other test chip waveguides. However, both chips were fabricated under the same conditions, so we expect the two chips to have similar performance metrics.

5. Conclusion and Future Work

With the test setup currently in place, we were able to couple light into the waveguides and take power measurements. However, with the data that we have taken so far, we cannot definitively make a conclusion on the performance of the fabricated chips with the lens structure in the silicon waveguide crosses. While initial data points to a 0.47dB insertion loss, the data is too inconsistent to draw any solid conclusions. Moreover, power coupled into the straight waveguides would vary considerably, pointing to a flaw in the test setup that needs to be addressed. To aid in coupling efficiency, we are waiting for a new camera that will aid in fiber alignment. Consistent fiber alignment will allow us to attain consistent coupling efficiency.

Another point to note is that the current fabricated devices are fabricated with electron-beam lithography. However, they do not account for the proximity effect that often plagues electron-beam lithography, where the etched pattern often does not match the intended etch pattern. Future device fabrication will account for the proximity effect to produce devices that more closely match the schematic outlined in the original paper. The inconsistency between the lenses aligned along the two directions are believed to be a result of the fracturing done in the software and we are currently working to resolve that through redefining how the system fractures the pattern.

6. Acknowledgements

The author would like to thank LTC Souhan for his tireless efforts in supporting this research. His guidance and patience made this research possible. The author would also like to thank LTC Kirk Ingold, as well as the other researchers at the Photonics Research Center, for their help during this research. This project was a success because of their advice and support.

7. References

[1] Y. Ma, Y. Zhang, S. Yang, A. Novack, R. Ding, A. Lim, G. Lo, T. Baehr-Jones, and M. Hochberg, “Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect,” Optics Express, vol. 21, no. 24, 2013.

[2] Y. Xie, J. Xu, and J. Zhang, “Elimination of cross-talk in silicon-on-insulator waveguide crossings with optimized angle,” Optical Engineering, vol. 50, no. 6, 2011.

[3] P. Sanchis, P. Villalba, F. Cuesta, A. Hakansson, A. Griol, J. Galan, A. Brimont, and J. Marti, “Highly efficient crossing structure for silicon-on-insulator waveguides,” Optics Letters, vol. 34, no. 18, 2009.

[4] Y. Zhang, S. Yang, A. Lim, G. Lo, C. Galland, T. Baehr-Jones, and M. Hochberg, “A CMOS-Compatible, Low-Loss, and Low-Crosstalk silicon Waveguide Crossing,” IEEE Photonics Technology Letters, vol 25, no. 5, 2013.

[5] M. Dai, Y. Xu, X. Yan, L. Ma, X. Liu, M. Lu, and Y. Chen, “An ultra-compact and highly efficient waveguide crossing for dense photonic integration,” Awaiting Publication

[6] M. Parikh, “Corrections to proximity effects in electron beam lithography,” Journal of Applied Physics, vol. 50, no. 6, 1979.