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Analytical Delay and Variations Modeling in the Subthreshold Region

Sungil Kim
Electrical and Computer Engineering
Auburn University
341 War Eagle Way
Auburn, Alabama 36849 USA

Faculty Advisor: Prof. Vishwani Agrawal

Abstract

Power constraint on modern electronics has been an increasingly significant part of VLSI design. Thus, subthreshold circuit design where the supply voltage is less than the device threshold voltage gained renewed attention to reduce the energy. However, such reduction comes with process, voltage, and temperature (PVT) variations. Furthermore, as previous analytical delay models (i.e. Alpha-power law MOSFET model) do not take account of these variations, their errors in subthreshold region are large. Therefore, this paper presents analytical delay model that considers PVT variations and models variations of analytical delay in the subthreshold region. The proposed model is verified through the simulation on PTM low power 16-nm technology (threshold voltage = 0.68V). Result shows that the proposed analytical delay model has a maximum error of 33.4% while Alpha-power law MOSFET model has a maximum error of 71.1% for 0 to 1 input transition over the range of 0.2V to 0.4V of supply voltage. In addition, three analytical delay variations are modeled and verified. In contrast to previous research, the proposed model considers the drain-induced barrier lowering (DIBL) effect. The accuracy is improved with a compensation factor and verified for the range of 0.15V to 0.4V of supply voltage along with threshold voltage variation up to 30mV, supply voltage variation up to 50mV, and temperature variation up to 20°C. By considering process variations, supply voltage, and temperature variations, we demonstrate the delay variations up to 4.31×. Result shows an average error of 1%, 14.6%, and 6.8% for PVT variations respectively. These results can further the applicability of subthreshold circuit for ultra-low-power electronics.

Keywords: Analytical Delay Model, Subthreshold Circuits, PVT Variations

1. Introduction

Concerns about power consumption and its management are important, particularly in modern ultra-low power electronics. In 1971, Meindl and Swanson [1] introduced subthreshold circuits—where the supply voltage is less than the device threshold—and provided the insight to the potential 10 to 1000 times improvement in power-speed product by using lower supply voltage. In the 1900s and 2000s, researchers proved the workability of subthreshold circuits. For instance, the feasibility of implementation of subthreshold CMOS circuits for low performance application has been proven, and the analysis of threshold voltage and temperature variations are carried [2]. The results from [3, 9] showed that the minimum energy operation occurs at the subthreshold region.

From the results of feasibility of subthreshold circuits, in the last decade, the ultra-low power systems attracted particular attention, such as circuits for biomedical sensing and monitoring [4]-[5], ultra-low po wer processors and memories [6]-[7], and energy harvesting and power management units [8]. For low- to moderate-speed systems whose primary interst is to reduce power consumption or that have a significant constraint on power consumption, operating at the subthreshold region can achieve the minimum energy operation [9]. While operating at subthreshold region significantly reduces the power consumption and can operate at the minimum energy, it introduces process, voltage, and temperature (PVT) variations [7] that directly affect circuit delay and performance. Therefore, analytical

delay models that do not carefully characterize these variations or were previously applicable to superthreshold circuits can no longer accurately model delay in the subthreshold region, and more accurate analytical models to characterize variations in the subthreshold region are needed.

For instance, the Alpha-power law MOSFET model [10] introduced a simple but practical MOSFET model and derived analytical expressions for the drain current, short-circuit power, logic threshold voltage, and propagation delay. In this paper, we focus on the analytical model for the propagation delay of CMOS inverter. While this model shows an average error of 0.55% from 0 to 1 input transition at $V_{DD} = 1V$ on the predictive technology model (PTM) 45-nm bulk CMOS technology [11], the maximum error in the subthreshold region is 46.12%. This error prompted some of the previous efforts to better model analytical delay in the subthreshold region.

Several analytical delay models were proposed for the subthrehsold region to characterize the increased variations and degraded device characteristics due to the reduced I_{on}/I_{off} [7] and the saturation current that exponentially depends on the gate and threshold voltages [12]. In particular, the model [13] present the analytical delay model for CMOS inverter, considering process variability and on-current transient variations, and simulate on the STM 45-nm technology. The model [14] develops PVT variations modeling and verify against CMOS 130-nm technology.

This paper derives three analytical delay variations modeling for the subthreshold region. In contrast to [14], the proposed model considers the drain-induced barrier lowering (DIBL) effect. While authors from [13] do not derive separate analytical variations model, we derive simple models to characterize PVT variations based on the analytical delay model developed from [13], improve the accuracy with a compensation factor, and verify for the range of $0.15 \leq V_{DD} \leq 0.4$ along with V_{DD} variation up to 50mV, V_{th} variation up to 30mV, and temperature variation up to 20ºC through the simulation on PTM low power 16-nm technology ($V_{th} = 0.68191$V) [11].

2. Analytical Delay Modeling

2.1. Alpha-Power Law MOSFET Model

The Alpha-Power law MOSFET model expresses drain current as follows:

$$I_D = \begin{cases} 0 & , V_{GS} \leq V_{th} \text{ (cutoff region)} \\ \left(\frac{I'_{D0}}{V'_{D0}}\right) V_{DS} & , V_{DS} < V_{DSAT} \text{ (linear region)} \\ I'_{D0} & , (V_{DS} \geq V_{DSAT} \text{ (saturation region)} \end{cases} \quad (1)$$

where

$$I'_{D0} = I_{D0}\left(\frac{V_{GS} - V_{th}}{V_{DD} - V_{th}}\right)^{\alpha}$$

$$V'_{D0} = V_{D0}\left(\frac{V_{GS} - V_{th}}{V_{DD} - V_{th}}\right)^{\alpha/2}$$

In the above equation, it is shown that the α-power law depends on V_{th} (threshold voltage), α (velocity saturation index), V_{D0} (drain saturation voltage), and I_{D0} (drain current). Voltage and current characteristics are shown in Figure 1.

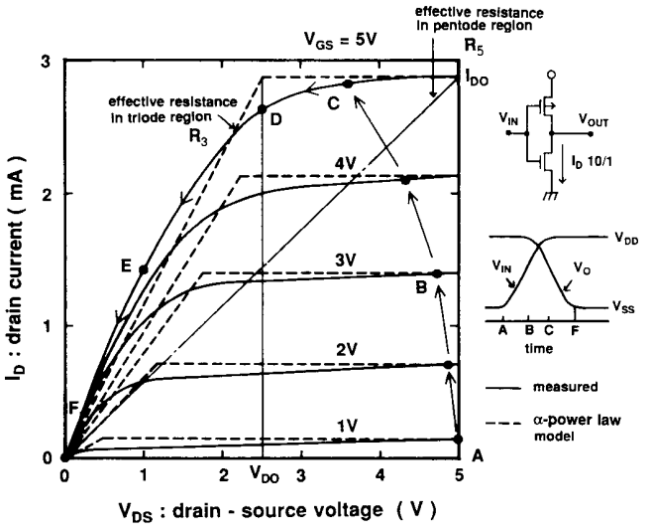

Figure 1. α–power law MOS model [10]

From the α-power law, the simple yet useful analyticla delay model for CMOS inverter is derived [10].

$$Delay \propto \frac{V_{DD}}{(V_{DD}-V_{th})^{\alpha}} \tag{2}$$

The authors [10] note that this model should not be used for VLSI operating in the near- and subthreshold region because of sensitivitiy to variations. Therefore, we verify errors of the α-power law in those regions and propose analytical delay model specifically for subthreshold circuits.

2.2. Proposed Analytical Delay Model

We consider the nominal inverter delay with the input transition from 0 to 1. The delay can be estimated by the time taken to charge and discharge the output node.

$$\text{Delay} = \frac{\text{Q}_{\text{output}}}{I_{on}} = \frac{KV_{DD}(C_L+C_{out})}{I_{leakage}} \tag{3}$$

$$\text{I}_{\text{leakage}} = I_0 \exp\left(\frac{\lambda V_{DS}}{mV_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{4}$$

$$\text{since} \quad \exp\left(-\frac{V_{DS}}{V_T}\right) \cong 0\,,\ \text{I}_{\text{leakage}} = I_0 \exp\left(\frac{\lambda V_{DS}}{mV_T}\right) = I_0 \exp\left(\frac{\lambda V_{DD}}{mV_T}\right) \tag{5}$$

$$\text{Delay} = \frac{\text{Q}_{\text{output}}}{I_{on}} = \frac{KV_{DD}(C_L+C_{out})}{I_0 \exp\left(\frac{\lambda V_{DD}}{mV_T}\right)} \tag{6}$$

C_L is an external capacitance, and C_{int} is internal subthreshold capacitance. λ is the DIBL coefficient in subthreshold region, m is the subthreshold slope factor, V_T is the thermal voltage ($V_T = \frac{kT}{q}$). Delay depends on the product of V_{DD} (supply voltage) and total capacitance.

2.3. Simulation Result

The CMOS inverter was implemented and simulated using the predictive technology model (PTM) low-power 16-nm technology [11] ($V_{th} = 0.68$V). For both NMOS and PMOS, the channel length of 50nm was used. For parameters (K, V_{th}, and α) used in the α-power law, HSPICE and MATLAB were used to extract values. After obtaining I-V characteritics through HSPICE, we ran the best-fit lines in MATLAB. Shown in Figure 2 and Table 1, the result shows the improvement in accuracy. Over the range of 0.2V to 0.4V of supply voltage, the average error of proposed model is 16.5% compared to 39.8% of the α-power law model. The worst-case occurs when supply voltage is 0.2V. Note that it is rare for subthreshold circuits to operate at that low voltage because of the performance degradation.

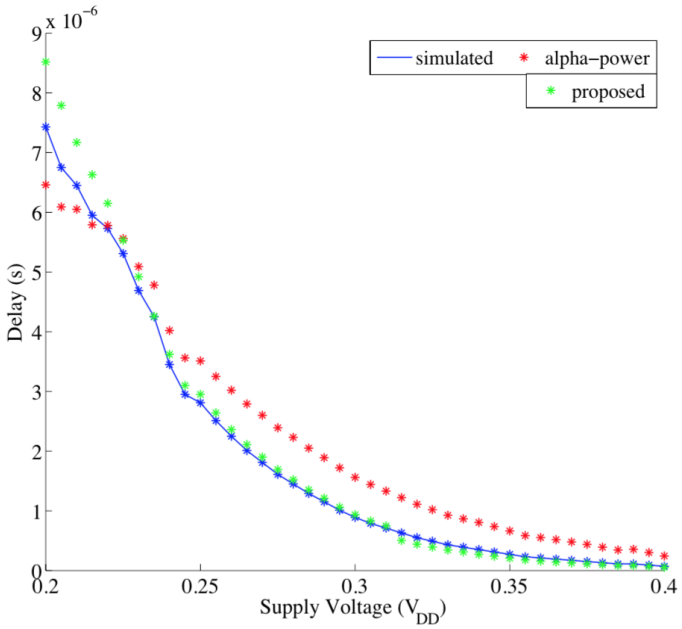

Figure 2. Accuracy of proposed model compared to the α-power law model

Table I. Average and worst cases for proposed model and the α-power law model

Error	α-power law	proposed
Average	39.8%	16.5%
Worst	71.1%	33.4%

3. Variations Modeling

3.1. Analytical Delay Model for Variations Analysis

We consider the nominal inverter delay with the input transition from 0 to 1. The subthreshold leakage current is expressed in [15]:

$$I_{\text{leakage}} = I_0 \exp\left(\frac{V_G - V_S - V_{T0} - \gamma V_S + \lambda V_{DS}}{m V_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right] \text{ where } I_0 = \mu C_{ox}\frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{GS} - V_{th}}{m V_T}\right). \quad (7)$$

γ is the linearized body effect coefficient, λ is the DIBL coefficient in subthreshold region, m is the subthreshold slope factor, V_T is the thermal voltage ($V_T = \frac{kT}{q}$), μ is the carrier mobility, C_{OX} is the oxide capacitance for the unit area. We ignore other exponential parameters other than $\frac{\lambda V_{DS}}{mV_T}$ in leakage current and get the following:

$$I_{\text{leakage}} = I_0 \exp\left(\frac{\lambda V_{DS}}{mV_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{th}}\right)\right]. \tag{8}$$

Previous research [14] derives the following propagation delay equation.by applying Equation (2) to CMOS inverter with an external capacitance load C_L and internal subthreshold capacitance C_{int} assuming 0 to 1 input transition.

$$Delay = ln2\left(\frac{2mV_T}{I_0\lambda^2 V_{DD}}\right)\left[\frac{\frac{\lambda V_{DD}}{2}+mV_T}{\exp\left(\frac{\lambda V_{DD}}{2mV_T}\right)} - \frac{\lambda V_{DD}+mV_T}{\exp\left(\frac{\lambda V_{DD}}{mV_T}\right)}\right](C_L + C_{int}) \tag{9}$$

On the basis of Equation (9), we conduct analysis of the PVT variations modeling in the subthreshold region.

3.2. Proposed Variations Models

3.2.1. effect of supply voltage (V_{DD}) variation

Supply voltage variation impacts the delay of subthreshold circuits. Let V_{DD1} as the nominal supply voltage and V_{DD2} as the varied supply voltage. $\Delta Delay$ indicates the variations in delay (i.e., 1 indicates no change in delay after cetain variation ,and 0.5 indicates the delay is reduced 50% from the nominal delay). From Equation (9), the following analytical delay model has been derived.

$$\begin{aligned}\Delta Delay_{\Delta V_{DD}} &= \frac{\tau_{step,V_{DD2}}}{\tau_{step2,V_{DD1}}} \\ &= \frac{V_{DD1}}{V_{DD2}}\frac{\left[\frac{\frac{\lambda V_{DD2}}{2}+mV_T}{\exp\left(\frac{\lambda V_{DD2}}{2mV_T}\right)} - \frac{\lambda V_{DD2}+mV_T}{\exp\left(\frac{\lambda V_{DD2}}{mV_T}\right)}\right]}{\left[\frac{\frac{\lambda V_{DD1}}{2}+mV_T}{\exp\left(\frac{\lambda V_{DD1}}{2mV_T}\right)} - \frac{\lambda V_{DD1}+mV_T}{\exp\left(\frac{\lambda V_{DD1}}{mV_T}\right)}\right]}\end{aligned} \tag{10}$$

Because $\exp\left(\frac{\lambda V_{DD}}{2mV_T}\right) \approx \exp\left(\frac{\lambda V_{DD}}{mV_T}\right)$, the above equation can be further reduced to the following:

$$\Delta Delay_{\Delta V_{DD}} = \exp\left[\frac{\lambda(V_{DD1} - V_{DD2})}{2mV_T}\right]. \tag{11}$$

This assumption that $\exp\left(\frac{\lambda V_{DD}}{2mV_T}\right) \approx \exp\left(\frac{\lambda V_{DD}}{mV_T}\right)$ is verified by simulating both equations, and the percent difference between the simplified equation and not simplified equation was negligible. The DIBL coefficent λ is given by the device. The subthreshold slope factor m can be calculated by Equation (6).

$$\text{m} = \ln(10)\,\text{V}_\text{T}\left(1 + \frac{\text{C}_\text{d}}{\text{C}_\text{ox}}\right) \tag{12}$$

where C_d is the depletion layer capacitance and C_{ox} is the gate-oxide capacitance.

Equation (11) shows that the delay variation exponentially depends on the supply voltage variation. It tends to underestimate the delay, and thus we consider the compensation factor suggested by [13]. After multiplying by $\frac{V_{DD2}}{V_{DD1}}$, we get Equation (13).

$$\Delta Delay_{\Delta V_{DD}} = \frac{V_{DD2}}{V_{DD1}} \exp\left[\frac{\lambda(V_{DD1} - V_{DD2})}{2mV_T}\right] \tag{13}$$

3.2.2. effect of temperature variation

The delay variations due to temperature variation can be written as Equation (7).

$$\Delta \mathrm{D}elay_{\Delta T} = \frac{\tau_{step,T2}}{\tau_{step2,T1}} = \frac{V_{T2} I_{0,T1}}{V_{T1} I_{0,T2}} \frac{\left[\frac{\frac{\lambda V_{DD}}{2} + mV_{T2}}{\exp\left(\frac{\lambda V_{DD}}{2mV_{T2}}\right)} - \frac{\lambda V_{DD} + mV_{T2}}{\exp\left(\frac{\lambda V_{DD}}{mV_{T2}}\right)}\right]}{\left[\frac{\frac{\lambda V_{DD}}{2} + mV_{T1}}{\exp\left(\frac{\lambda V_{DD}}{2mV_{T1}}\right)} - \frac{\lambda V_{DD} + mV_{T1}}{\exp\left(\frac{\lambda V_{DD}}{mV_{T1}}\right)}\right]} \tag{14}$$

The variation in temperature directly affects I_0 due to the changes in μ and V_T. The change in temperature also directly influences V_{th}. Therefore, the impact of the change on μ and V_{th} is modeled using the mobility temperature exponent (UTE) and the temperature coefficient for V_{th} (K_{th1}) for BSIM4 level-54 model. Previous research by Lin et al. [13] shows the temperature effects on μ and V_T as follows:

$$\mu_2 = \mu_1 \left(\frac{T_2}{T_1}\right)^{UTE} \tag{15}$$

$$V_{th2} = V_{th1} + K_{th1}\left(\frac{T_2}{T_!} - 1\right). \tag{16}$$

Since $\exp\left[\frac{V_{GS} - V_{th1}}{mV_{T1}} - \frac{V_{GS} - V_{th2}}{mV_{T2}}\right] \cong 0$,

$$\frac{I_{0,T1}}{I_0,T2} = \left(\frac{V_{T1}}{V_{T2}}\right)^2 \left(\frac{T_1}{T_2}\right)^{UTE} \tag{17}$$

Using Equations (15) and (17), Equation (14) can be written as follows:

$$\Delta \mathrm{D}elay_{\Delta T} = \left(\frac{V_{T1}}{V_{T2}}\right)\left(\frac{T_1}{T_2}\right)^{UTE} \frac{\left[\frac{\frac{\lambda V_{DD}}{2} + mV_{T2}}{\exp\left(\frac{\lambda V_{DD}}{2mV_{T2}}\right)} - \frac{\lambda V_{DD} + mV_{T2}}{\exp\left(\frac{\lambda V_{DD}}{mV_{T2}}\right)}\right]}{\left[\frac{\frac{\lambda V_{DD}}{2} + mV_{T1}}{\exp\left(\frac{\lambda V_{DD}}{2mV_{T1}}\right)} - \frac{\lambda V_{DD} + mV_{T1}}{\exp\left(\frac{\lambda V_{DD}}{mV_{T1}}\right)}\right]}. \tag{18}$$

After adding compensation factor of $\left(\frac{T_1}{T_2}\right)^2$, we have

$$\Delta \mathrm{D}elay_{\Delta T} = \left(\frac{V_{T1}}{V_{T2}}\right)\left(\frac{T_1}{T_2}\right)^{UTE+3} \frac{\left[\frac{\frac{\lambda V_{DD}}{2} + mV_{T2}}{\exp\left(\frac{\lambda V_{DD}}{2mV_{T2}}\right)} - \frac{\lambda V_{DD} + mV_{T2}}{\exp\left(\frac{\lambda V_{DD}}{mV_{T2}}\right)}\right]}{\left[\frac{\frac{\lambda V_{DD}}{2} + mV_{T1}}{\exp\left(\frac{\lambda V_{DD}}{2mV_{T1}}\right)} - \frac{\lambda V_{DD} + mV_{T1}}{\exp\left(\frac{\lambda V_{DD}}{mV_{T1}}\right)}\right]}. \tag{19}$$

The value of UTE for the chosen technology is -1.5. The result in 4 shows estimated delays from both Equation (18) and (19) and demonstrates that compensation factor significantly increases the accuracy of the delay variation model.

3.2.3. effect of process variation

Process variations include variations in threshold voltage, effective channel length, doping concentration, and more parameters. Since threshold voltage variation is a dominant factor affecting the delay in the subthreshold region [16], the following model considers only the variations in V_{th}.

$$\Delta Delay_{\Delta V_{th}} = \frac{\tau_{step,V_{th1}}}{\tau_{step2,V_{th2}}} = \frac{I_{0,V_{th1}}}{I_{0,V_{th2}}} = \exp\left[\frac{V_{th2}-V_{th1}}{mV_T}\right] \quad (20)$$

Note that the Equation (20) is unchanged from the previous model developed by [13].

4. Simulation Results

The CMOS inverter was implemented and simulated using the predictive technology model (PTM) low-power 16-nm technology [11] ($\lambda = 0.1, m \cong 0.05916$ at $T = 25$ °C). For both NMOS and PMOS, the channel length of 50nm was used.

With the load capacitance of 1aF and the 0 to 1 step input, the inverter delay has been simulated @ $T = 25$ °C. Figure 3. shows the simulated and estimated inverter delay variations by Equation (6) due to the supply voltage variation. The maximum delay variation of up to 4.31× is found when $V_{DD} = 0.38V, \Delta V_{DD} = 50mV$. The minimum error of 0.1% and maximum error of 79.1% are found at $V_{DD} = 0.17V, \Delta V_{DD} = 50mV$ and $V_{DD} = 0.225V, \Delta V_{DD} = 30mV$ respectively. Note that in this technology, the percent error is greater than less scaled technology (i.e. 130-nm). Therefore, we also compare this result with the previously developed model [13]. For the worst-case of 4.31× delay variations, the proposed model is ~100% more accurate as the previous model [13] does not consider DIBL effect.

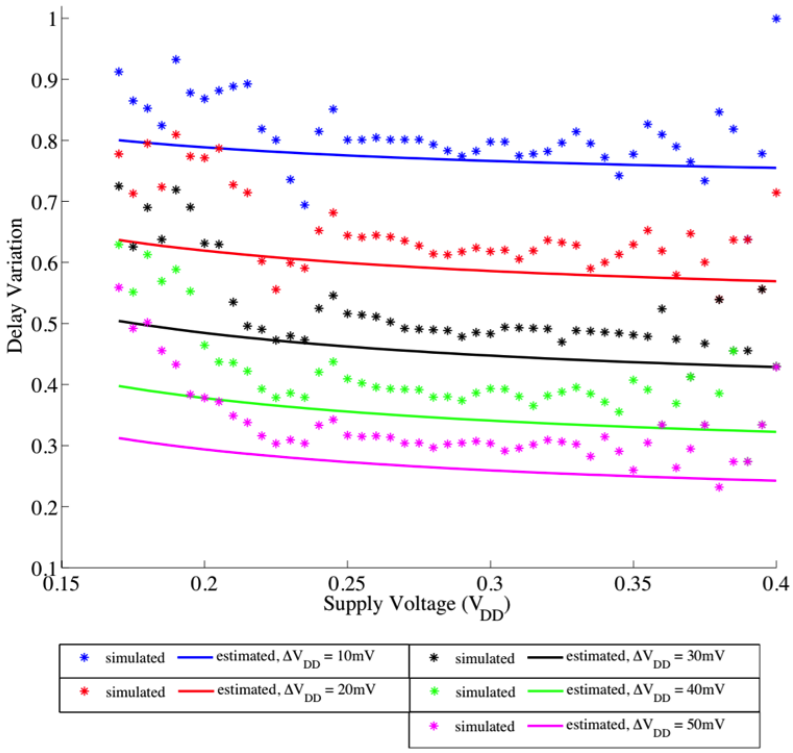

Figure 3. Simulated vs. estimated inverter delay with compensation factor V_{DD}variations @ T = 25 °C

Figure 4 shows the simulated and estimated inverter delay variations by Equation (12) due to temperature variation. The CMOS inverter is simulated at different temperature from $\Delta T = 5 - 20$ ºC. From $V_{DD} = 0.15 - 0.4V$, the maximum delay variation of up to 1.88× is found when $V_{DD} = 0.225V, \Delta T = 20$ ºC. The maximum error of 37.9% is found at $V_{DD} = 0.175V, \Delta T = 5$ ºC. For greater temperature variations such as $\Delta T \geq 40$ ºC, the average error exceeds 31% with a worst-case of 41%.

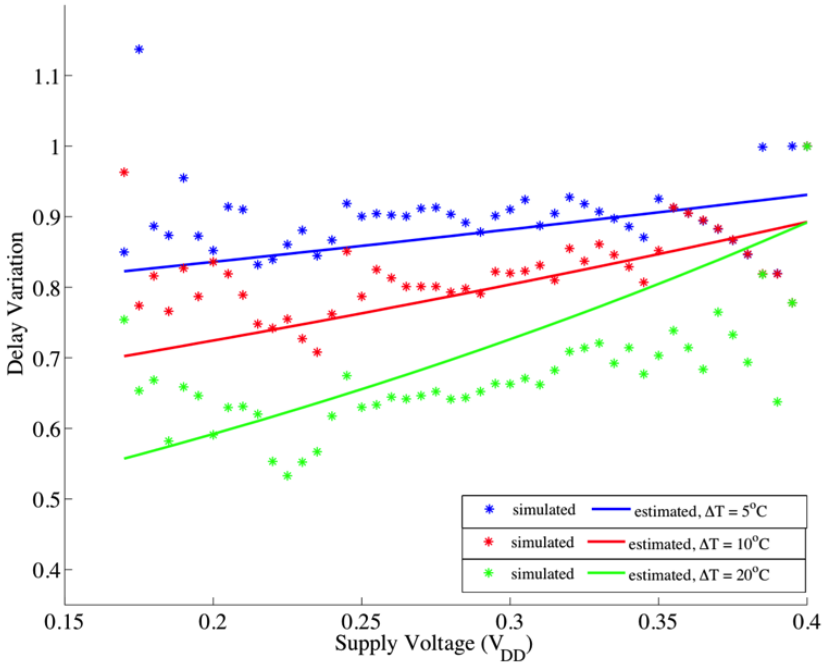

Figure 4. Simulated vs. estimated inverter delay with compensation factor with temperature variation

Figure 5 compares the simulated and estimated inverter delay variations by Equation (13) due to the process variation. We assume a normal distributino of V_{th} and run Monte Carlo simulations (1000 runs) for the given $\Delta V_{th} = 10mV - 30mV$. The proposed model estimates with an average error of 1%, minium error of 0%, and maximum error of 6%. The worst case occurs at $V_{DD} = 0.38V, \Delta V_{th} = 30mV$. We observed that for $\Delta V_{th} \geq 30mV$, the proposed model tends to underestimate the delay. It is partly because the DIBL coffieicnt, λ, changes near the threshold voltage (i.e. from 0.1 to 0.001 for the chosen technology).

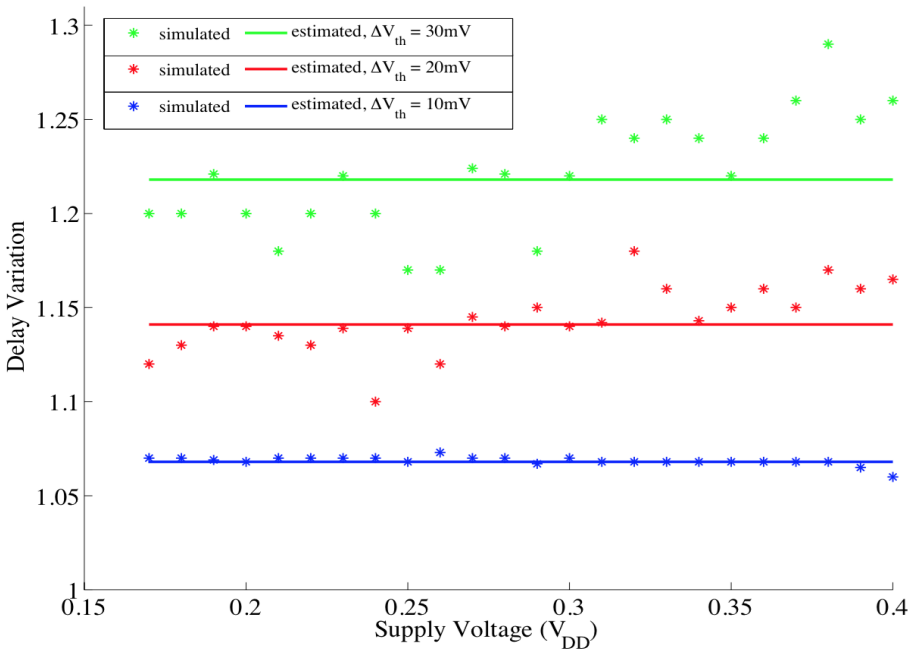

Figure 5. Simulated vs. estimated inverter delay with V_{th} variations

Table 2 shows the effect of compensation factor for two models that correspond to supply voltage and temperature variations. The result shows that the compensation factor greatly enhances the accuracy of estimation of delay and variations.

Table 2. Average, best, and worst cases for models with and without the compensation factor

Error	Eq. (5)	Eq. (6) with compensation factor	Eq. (11)	Eq. (12) with compensation factor
Average	27.4%	14.6%	62.1%	6.8%
Best Case	0.4%	0.1%	20.2%	0.1%
Worst Case	131.7%	79.1%	87.5%	37.9%

5. Conclusion

Accurately measuring analytical delay is important for efficient circuits, and it still remains challenging for subthreshold CMOS circuits due to PVT (process, voltage, and temperature) variations.

In this paper, we derive and propose analytical dealy model and three PVT variations models for subthreshold CMOS circuits. The result shows that proposed delay model has an average error of 16.5% compared to an average error of 39.8% of the alpha-power law model. We also found the delay variations up to 4.31×, 1.29×, and 1.88× for the choosen range of V_{DD}, V_{th}, and temperature. We verify our proposed model on simulation using PTM low power 16-nm technology [11] and demonstrated that proposed delay variations models estimate with the maximum errors of 79.1%, 37.9%, and 6% for supply voltage, threshold voltage, and temperature variations respectively. The proposed delay variations models can be used to predict circuits' behaviors and functions in sensitive and extreme environments. Compared to the previous model [13], this model considers the DIBL effect, and compared to [14], this paper presents three separate, compact models to characterize V_{DD}, V_{th}, and temperature variations and considers adding a compensation factor.

6. References

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